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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/005,627	12/04/2001	Nai-Shung Chang	JCLA6879	8225

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EXAMINER	
CHEN, TSE W	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 04/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/005,627	CHANG ET AL.	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 8-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment dated March 30, 2005.

2. Claims 1-6 and 8-16 are presented for examination. Applicant has canceled claim 7.

Claim Rejections - 35 USC § 112

3. Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Specifically, Applicant fails to disclose how a plurality of switches with claimed connections are able to control the connections between the termination resistors and the voltage source when the plurality of switches are located between the plurality of termination resistors and the memory slot. The Examiner submits that it would require undue experimentation for one of ordinary skill in the art to make and use the invention for the reason set forth hereinabove. To proceed with prosecution, Examiner will assume that a switch is supposed to control the connection between the a memory module and a terminal resistor.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 8-13 and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fan, US Patent 6665736, in view of Taguchi, US Patent 6480030.

6. In re claim 8, Fan discloses a motherboard [300], comprising [fig.3a]:

- A memory module slot [303] for receiving a memory module [305].
- A plurality of termination resistors [array of Rt's], coupled to the memory module slot [fig.3a; col.5, ll.1-22; col.2, ll.18-43].
- A controller chip set [301], coupled to the memory module slot to provide a control signal [col.1, ll.28-40; 301 directs access to memory modules with control signals traveling through memory module slot to terminating Rt], and wherein in connection, the plurality of termination resistors [Rt's] are coupled to the memory module [305] in the memory module slot [303] [col.2, ll. 18-43; 305 must be inserted into 303 which would effectively couple 305 to the Rt's].

7. Fan did not discuss reducing power consumption.

8. Taguchi discloses a configuration with reduced power consumption [col.2, ll.50-54], comprising:

- A plurality of termination resistors [Rt may embody a plurality of resistors as one with ordinary skill in the art can easily configure according to Kirchoff's Law] [fig.2; col.5, ll.9-48].
- A switch [21], coupled between a plurality of termination resistors [Rt] and a voltage source [Vtt], on/off of the switch being controlled by a control signal [32] [col.5, ll.33-48].

- A controller chip set [23], coupled to the switch to provide the control signal [col.5, l.49 – col.6, l.41; 23 sends control signal to 32-34 representing the switches], wherein when the configuration enters a power saving mode [low speed mode] or when the memory module is not inserted in the memory module slot, the control signal commands the switch to cut off the connection between the termination resistors and the voltage source [col.5, ll.33-48].

9. It would have been obvious to one of ordinary skill in the art, having the teachings of Fan and Taguchi before him at the time the invention was made, to modify the motherboard taught by Fan to include the teachings of Taguchi in order to obtain the claimed motherboard with reduced power consumption. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to reduce power consumption [Taguchi: col.1, l.65 – col.2, l.11; col.2, l.50 – col.3, l.2; col.5, ll.33-48].

10. As to claim 9, the Examiner has taken Official Notice that it is well known in the art to have a control signal that includes a clock enable signal.

11. As to claim 10, Fan discloses, wherein the memory module comprises a double data rate dynamic random access memory (DDR DRAM) [305; col.1, ll.41-67].

12. As to claim 11, the Examiner has taken Official Notice that it is well known in the art to have a motherboard be used in a laptop computer.

13. As to claim 12, Fan discloses, wherein the controller chip set comprises a north bridge chip [301].

14. In re claim 13, Fan discloses an operation method of a motherboard [300], wherein the motherboard comprises a memory module slot [303] for receiving a memory module [305] and a

plurality of termination resistors [array of Rt's], the termination resistors and a voltage source [Vtt] form an operation circuit [fig.3a; col.5, ll.1-22; col.2, ll.18-43], the operation method comprising:

- Using a control signal [on] to establish a connection between the memory module and the operation circuit when the motherboard enters a normal operation mode and when the memory module slot is inserted with the memory module [motherboard operates normally when turned on with memory module in slot].

15. While Taguchi discloses an operation method of a configuration with reduced power consumption [col.2, ll.50-54], the operation method comprising [fig.2; col.5, ll.9-48]:

- Using a control signal to cut off a connection between a module [23] and an operation circuit [Vtt, Rt] when the configuration enters a power saving mode [low speed mode] [open switch].
- Using the control signal to establish the connection between the module and the operation circuit when the configuration enters a normal operation mode [high speed mode] [close switch].

16. It would have been obvious to one of ordinary skill in the art, having the teachings of Fan and Taguchi before him at the time the invention was made, to modify the motherboard taught by Fan to include the teachings of Taguchi in order to obtain the claimed motherboard with reduced power consumption, particularly relating to using a control signal to control the connection between a memory module [Fan: 305] and an operation circuit [Fan: Vtt, Rt]. One of ordinary skill in the art would have been motivated to make such a combination as it provides a

way to reduce power consumption [Taguchi: col.1, l.65 – col.2, l.11; col.2, l.50 – col.3, l.2; col.5, ll.33-48].

17. As to claim 15, Taguchi discloses, wherein the cutting off step comprises a step of cutting off connections between the termination resistors and the voltage source [fig.2; col.5, ll.33-48].

18. As to claim 16, the Examiner has taken Official Notice that it is well known in the art to have a control signal that includes a clock enable signal provided by a laptop computer.

19. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fan in view of Taguchi and Takagi et al., US Patent 6356096, hereinafter Takagi.

20. In re claim 1, Fan discloses a motherboard [300], comprising [fig.3a]:

- A memory module slot [303] for receiving a memory module [305] therein.
- A DDR (Double data rate) termination array [array of Rt's corresponding to signal lines; col.5, ll.1-22], coupled between the memory module slot and a voltage source, comprising a plurality of termination resistors [array of Rt's] connected to the voltage source [Vtt] [col.2, ll.18-43].
- A controller chip set [301], coupled to the memory module slot and the DDR termination array, providing a control signal [col.1, ll.28-40; 301 directs access to memory modules with control signals traveling through memory module slot to terminating Rt] and wherein in connection, the plurality of termination resistors [Rt's] are coupled to the memory module [305] in the memory module slot [303] [col.2, ll. 18-43; 305 must be inserted into 303 which would effectively couple 305 to the Rt's].

21. Fan did not discuss reducing power consumption.

22. Taguchi discloses a configuration with reduced power consumption [col.2, ll.50-54], comprising:

- A termination array [21, 22 with associated circuitries] comprising a plurality of termination resistors [Rt] connected to the voltage source [Vtt] and a plurality of switches [21, 22], wherein the plurality of switches controlling connections between a module slot [23] and the termination resistors [Rt] are controlled according to a control signal [col.5, ll.33-48].
- A controller chip set, providing the control signal, [inherently, a controller chip set in the broadest interpretation is needed to issue a control signal], wherein when the configuration enters a power saving mode [low speed mode], the control signal cuts off the connections between the termination resistors [Rt] and the voltage source [Vtt] [col.5, ll.33-48], and wherein in connection, the plurality of termination resistors [Rt] are coupled to a module [inherently, a module in the broadest interpretation is coupled to 23 in order to receive the signal from 20] in the module slot [23] through the plurality of switches [21, 22] [fig.2].

23. It would have been obvious to one of ordinary skill in the art, having the teachings of Fan and Taguchi before him at the time the invention was made, to modify the motherboard taught by Fan to include the teachings of Taguchi in order to obtain the claimed motherboard with reduced power consumption. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to reduce power consumption [Taguchi: col.1, l.65 – col.2, l.11; col.2, l.50 – col.3, l.2; col.5, ll.33-48].

24. Fan and Taguchi did not disclose explicitly the specific configuration of having a switch connected between a termination resistor and the memory module slot.

25. Takagi discloses a termination array [102f; col.20, ll.41-48], comprising a termination resistor [150] connected to the voltage source [151] and a switch [156] between the termination resistor and a module slot [105] [fig.19; col.20, ll.30-35].

26. It would have been obvious to an ordinary artisan to utilize the specific configuration for the connection amongst the switches, resistors, and a module slot as taught by Takagi because Applicant has not disclosed an advantage, a particular purpose, or solution to a stated problem for the specific configuration. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with the specific configuration as taught by Taguchi because the Applicant's invention is intended to conserve power by cutting the connection to a voltage source, irrelevant of the termination resistor location.

27. As to claim 2, the Examiner has taken Official Notice that it is well known in the art to have a control signal that includes a clock enable signal.

28. As to claim 3, Fan discloses, wherein the memory module comprises a double data rate dynamic random access memory (DDR DRAM) [305; col.1, ll.41-67].

29. As to claim 4, the Examiner has taken Official Notice that it is well known in the art to have a motherboard be used in a laptop computer.

30. As to claim 5, Fan discloses, wherein the controller chip set comprises a north bridge chip [301].

31. As to claim 6, Fan discloses, wherein the DDR termination array comprises a plurality of signal terminals [inherently, signal terminals in the broadest interpretation is needed in order to

facilitate transfer of signals], coupled to the memory module slot [signal lines corresponding to data bus of DIMM] [col.2, ll. 27-42; col.5, ll.10-22] while Taguchi discloses, a signal terminal [10; a signal terminal in the broadest interpretation can be any point on a bus] coupled between a module slot [23] and a switch [21].

32. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fan and Taguchi as applied to claim 13 above, and further in view of Wallace, US Patent 5635852.

33. Fan and Taguchi disclose each and every limitation of the claim as discussed above in reference to claim 13. Fan and Taguchi did not disclose explicitly cutting off connection between the resistors and the memory module slot.

34. Wallace discloses the operation wherein the cutting off step comprises a step of cutting off connections between the termination resistor [740] and the slot [cell 700] [col.4, l.40 – col.5, l.17; col.6, ll.44-65].

35. It would have been obvious to one of ordinary skill in the art, having the teachings of Wallace, Fan and Taguchi before him at the time the invention was made, to modify the motherboard taught by Fan and Taguchi to include the teachings of Wallace in order to obtain the operation wherein the cutting off step comprises a step of cutting off connections between the termination resistors and the memory module slot. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to reduce power consumption [Taguchi: col.1, l.65 – col.2, l.11; col.2, l.50 – col.3, l.2; col.5, ll.33-48; Wallace: col.6, ll.44-65].

Response to Arguments

36. All rejections of claim limitations as filed prior to Amendment dated March 30, 2005 not argued in entirety or substantively in response filed as said Amendment have been conceded by Applicant and the rejections are maintained from henceforth.

37. Applicant's arguments with respect to claims 1 and 8 have been considered but are moot in view of the new ground(s) of rejection.

38. All other claims were not argued separately.

Conclusion

39. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tse Chen
April 25, 2005

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
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